

JCS/579

	Class	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

**U.S. UTILITY Patent Application**

U.S. OFFICE FILE NO.	OL.P.E.	PATENT DATE
5	11/13/31	11/13/31

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/987012	F	257	758	2811 2815	<i>[Signature]</i>

APPLICANTS Kenichi Watanabe *Chu*

TITLE Semiconductor wafer device having separated conductive patterns in peripheral area and its manufacture method

PTO-20  
12/99

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>					
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.			
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		<b>NOTICE OF ALLOWANCE MAILED</b> _____ _____					
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ _____ _____	_____ (Primary Examiner)		<b>ISSUE FEE</b> <table border="1" style="width: 100%;"> <tr> <td style="text-align: center;">Amount Due</td> <td style="text-align: center;">Date Paid</td> </tr> <tr> <td style="height: 40px;"></td> <td></td> </tr> </table>		Amount Due	Date Paid		
Amount Due	Date Paid							
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		<b>ISSUE BATCH NUMBER</b> _____					

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